

What is claimed is:

1. A method of fabricating a local interconnection comprising:
forming a selective epitaxial growth seed layer pattern on a region of a
semiconductor substrate where a local interconnection is to be formed;
forming a selective epitaxial layer by performing epitaxial growth on the resultant
structure; and
reducing a resistance of the selective epitaxial layer to complete the local
interconnection.

2. The method of claim 1, further comprising, prior to forming the selective
epitaxial growth seed layer pattern:
forming a shallow trench isolation structure on the semiconductor substrate to
define an active region;
forming a gate on the active region; and
forming a spacer on a sidewall of the gate, and
wherein forming the selective epitaxial growth seed layer pattern comprises
forming the selective epitaxial growth seed layer pattern on the shallow trench isolation
structure, and forming the selective epitaxial layer comprises forming the selective
epitaxial layer on the active region, the selective epitaxial growth seed layer pattern,
and the gate, and
wherein the local interconnection comprises a local interconnection for
connecting a source/drain region of a transistor to a source/drain region of an adjacent
transistor.

3. The method of claim 1, further comprising, prior to forming the selective
epitaxial growth seed layer pattern:
forming shallow trench isolation structure on the semiconductor substrate to
define an active region;
forming first and second adjacent gates on the active region;
forming a spacer on sidewalls of the first and second gates; and

forming an insulating layer pattern for exposing an active region adjacent the first gate and exposing the second gate, and

wherein forming the selective epitaxial growth seed layer pattern comprises forming the selective epitaxial growth seed layer pattern on the insulating layer pattern, and forming the selective epitaxial layer comprises forming the selective epitaxial layer on the active region adjacent the first gate, the selective epitaxial growth seed layer pattern, and the second gate, and

wherein the local interconnection comprises a local interconnection for connecting a source/drain region of a transistor to a gate of an adjacent transistor.

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4. The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by implanting ions into the selective epitaxial layer.

15 5. The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises reducing the resistance of the selective epitaxial layer by siliciding the selective epitaxial layer.

6. The method of claim 1, wherein reducing the resistance of the selective epitaxial layer to complete the local interconnection comprises:
implanting ions into the selective epitaxial layer; and
siliciding the selective epitaxial layer.

20 7. The method of claim 1, wherein the selective epitaxial growth seed layer pattern comprises an $\text{Si}_x\text{O}_y\text{N}_z$ layer pattern.

8. The method of claim 7, wherein the selective epitaxial growth seed layer pattern comprises an $\text{Si}_x\text{O}_y\text{N}_z$ layer pattern, and wherein x is 55, y is 15, and z is 30.

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